Low Voltage CMOS Bandgap References with Temperature Compensated Reference Current Output

Edward K.F. Lee
Alfred Mann Foundation, 25134 Rye Canyon Loop, Suite 200, Santa Clarita, CA, USA
edl@aemf.org

ABSTRACT

Techniques for designing low voltage bandgap references providing both reference voltage and current outputs are proposed. By modifying the bandgap load or the bandgap core, the temperature dependences of the voltage output and the current output can be compensated separately. Based on the proposed techniques, a 1V bandgap reference was designed in a conventional 0.18µm CMOS process. Opamp was not required in this design. The current consumption was 7.1µA. It achieved temperature coefficients of < 21ppm/^{o}C and < 45ppm/^{o}C for the voltage output and the current output, respectively, over different temperature, process, and sheet resistance variations.

1. Introduction

Voltage reference circuit is one of the most important analog building blocks required in many circuits such as voltage regulators and analog-to-digital converters, etc. Most voltage references are designed based on a bandgap reference, which typically provides a well-defined, stable voltage over process, temperature and power supply variations. To achieve low voltage (LV) operations for advanced CMOS processes as well as for portable applications, low-power bandgap reference design techniques with sub-1V supply voltage have been developed [1-3]. In addition to voltage reference circuits, current reference circuits are also required in many sensor and biomedical applications (e.g. [4][5]) as well as for providing biasing for different mixed signal circuits. A current reference can be generated from the bandgap voltage using a resistor, a MOSFET and an opamp as shown in Fig. 1. To achieve a current output that is accurate and independent of temperature, an external temperature stable resistor can be used. Nevertheless, additional die area and power consumption are required for the opamp. Alternatively, dedicated temperature compensated current reference circuits (e.g. [6-8]) suitable for implementing in CMOS processes can also be used. The inaccuracy of the current output due to process variations can be trimmed or calibrated. Nevertheless, a separated voltage reference circuit and a separated current reference circuit are still required, leading to increases in area and power consumption. In this paper, design techniques for generating a temperature compensated reference current output from a LV bandgap reference are proposed. Since a single circuit is used for generating both reference voltage and current outputs, area and power consumptions can be minimized.

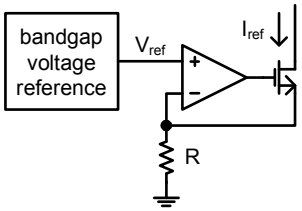

Fig. 1: Typical current reference generation

2. Typical LV CMOS Bandgap Reference

A typical LV CMOS bandgap reference [2] is shown in Fig. 2. Due to the feedback loop that consisted of the opamp, R_2, R_3, M_3 and M_4, the voltage across R_1 is equal to the difference between V_{EB1} and V_{EB2}, given as ΔV_{EB}. ΔV_{EB} can be written as $V_t \cdot \ln(N)$ where $V_t = kT/q$ and N is equal to the emitter area ratio of Q_2 and Q_1. Assuming that the W/L ratios of $M_3 - M_5$ are the same, the current, I, in the bandgap core (BGC) can be derived as

$$I = \frac{1}{R_2 + R_3}\left(V_{EB1} + \frac{R_2 + R_3}{R_1}\Delta V_{EB}\right) \quad (1)$$

The reference voltage output, V_{ref}, can be written as

$$V_{ref} = \frac{R_4}{R_2 + R_3}\left(V_{EB1} + \frac{R_2 + R_3}{R_1}\Delta V_{EB}\right) \quad (2)$$

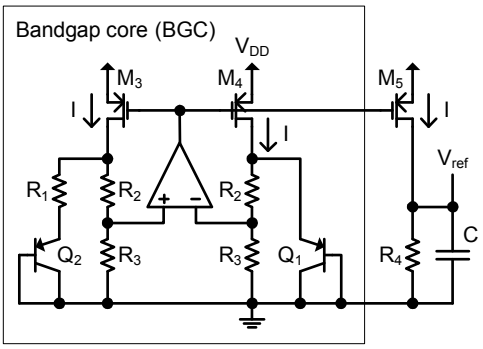

Fig. 2: Typical LV bandgap using an opamp

With proper selection of $(R_2+R_3)/R_1$, the negative temperature coefficient of V_{EB1} cancels out the positive temperature coefficient of ΔV_{EB} and V_{ref} has relatively small temperature dependence. However, due to the temperature coefficients of R_2 and R_3 (to be denoted by TC_R) the current, I, cannot be temperature compensated independently without affecting V_{ref}.

Nevertheless, the input common mode voltage of the opamp is shifted to a lower value by R_2 and R_3 and is given by $V_{EB1}\cdot R_3/(R_2 + R_3)$. A PMOS opamp input stage can be used and the supply voltage requirement for the opamp can be reduced. Therefore, sub-1V operation is possible.

3. LV Bandgap Reference with Modified Load

By taking the derivative of eqn. 1 with respect to temperature and setting it to zero at a reference temperature, T_0 (in ^oK), the current I(T) inside the BGC of Fig. 2 can have a zero temperature dependence at $T = T_0$ if the following condition is met

$$TC_R = \frac{1}{(R_2+R_3)I(T_0)}\left(\left.\frac{\partial V_{EB1}}{\partial T}\right|_{T=T_0} + \frac{R_2+R_3}{R_1}\frac{k\ln(N)}{q}\right) \quad (3)$$

This is achieved by adjusting the values of the resistors. In this case, the term in the parenthesis of eqn. 2 will not be zero temperature dependent at $T = T_0$. To generate a zero temperature dependent V_{ref} at $T = T_0$, the resistor load R_4 in Fig. 2 can be modified as shown in Fig. 3. Using this load, V_{ref} can be written as

$$V_{ref} = \frac{R_y}{R_x+R_y}V_{EB3} + \left(\frac{R_xR_y}{R_x+R_y}+R_z\right)I(T) \quad (4)$$

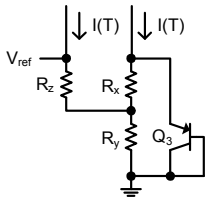

Fig. 3: Modified load for replacing R_4 in Fig. 2

Since I(T) is generated from the BGC according to eqn. 3, it has a zero temperature dependence at $T = T_0$ and V_{ref} will have a zero temperature dependence at $T = T_0$ when the following condition is satisfied.

$$I(T_0)\left(R_z+\frac{R_xR_y}{R_x+R_y}\right)TC_R + \frac{R_y}{R_x+R_y}\left.\frac{\partial V_{EB3}}{\partial T}\right|_{T=T_0} = 0 \quad (5)$$

Since V_{EB} has approximately $-2mV/^oK$ temperature dependence, TC_R is required to be positive in order to satisfy the above condition with proper selection of R_x, R_y and R_z. Note that the resistors with a positive TC_R such as diffusion resistors and well resistors are commonly found in a typical CMOS process. Therefore, a bandgap reference with temperature compensated current output can be realized using the technique proposed above.

4. Modified LV Bandgap Core

It can be observed that the topology of the modified load shown in Fig. 3 has similar connections as Q_1, R_2 and R_3 found in Fig. 2. Based on this observation, a new technique that merges the modified load into the BGC is proposed. The resulting bandgap reference is shown in Fig. 4. Assume that $I_{ref} = I$, I_{ref} and V_{ref} can be written as

$$I_{ref} = \frac{1}{R_2+2R_3}\left(V_{EB1} + \frac{R_2+R_3}{R_1}\Delta V_{EB}\right) \quad (6)$$

$$V_{ref} = \frac{R_4+2R_3}{R_2+2R_3}\left(V_{EB1} + \frac{R_2}{R_1}\Delta V_{EB}\right) \quad (7)$$

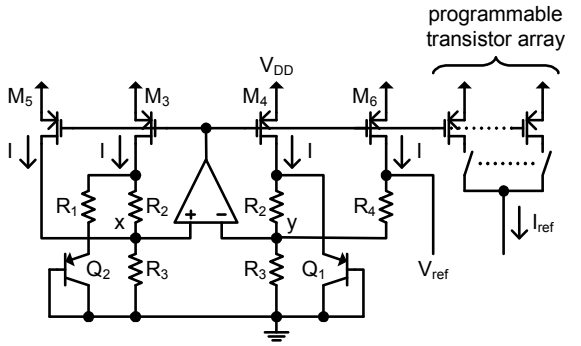

Fig. 4: Opamp based LV bandgap with I_{ref} output

From Eqn. 6 and 7, the proposed bandgap has two different temperature dependence terms (inside the parentheses) for temperature compensating I_{ref} and V_{ref}. The condition at which both I_{ref} and V_{ref} will have a zero temperature dependence at $T = T_0$ is given by

$$TC_R = \frac{1}{(R_2+2R_3)I(T_0)}\frac{R_3}{R_1}\frac{k\ln(N)}{q} \quad (8)$$

$$\left.\frac{\partial V_{EB1}}{\partial T}\right|_{T=T_0} = -\frac{R_2}{R_1}\frac{k\ln(N)}{q} \quad (9)$$

For resistors with a positive TC_R, the above conditions can be satisfied by proper selection of R_1, R_2 and R_3. Since a smaller number of resistors and bipolar transistors are required, the proposed bandgap has smaller area and current consumption, comparing to the bandgap discussed in Section 3.

The exact value of I_{ref} is determined by the values of the resistors even though it is temperature compensated. If an absolute accuracy is required, I_{ref} can be calibrated to the desired value using a programmable transistor array (PTA) to compensate for the current

changes due to variations on the sheet resistance. The PTA is similar to that used in realizing a current DAC. Hence, I_{ref} can be written as $I_{ref} = K \cdot I$ where K is a constant determined by the value set on the PTA after calibration.

5. Modified Bandgap without Using Opamp

To achieve low power dissipation, a LV bandgap voltage reference without an opamp was proposed in [3]. A temperature compensated reference current output can also be obtained from this bandgap with some modifications (Fig. 5). A circuit branch consisted of M_{4a} and R_4 is added between V_{DD} and node y of the bandgap reference proposed in [3]. Similar to the bandgap shown in Fig. 4, there are two currents flowing from nodes a and b to nodes x and y as shown in Fig. 5. Each current is equal to $s \cdot I$, where s is a scaling factor. Since the two bandgaps are similar in principle, except for the feedback loop, they share similar properties. Note that part of the current $s \cdot I$ flowing through M_2 and M_4 in the original bandgap proposed in [3] is now flowing through M_{4a} and R_4. This current is equal to $s \cdot k_2 \cdot I$ where k_2 is a constant less than one. After some analyses, I_{ref} and V_{ref} of the modified bandgap can be determined as

$$I_{ref} = \frac{1}{R_2 + (1+s)R_3}\left(V_{EB1} + \frac{R_2 + R_3}{R_1}\Delta V_{EB}\right) \quad (10)$$

$$V_{ref} = \frac{sk_2R_4 + (1+s)R_3}{R_2 + (1+s)R_3}\left(V_{EB1} + G\Delta V_{EB}\right) \quad (11)$$

$$G = \frac{sk_2R_4(R_2 + R_3) + sR_2R_3}{R_1[sk_2R_4 + (1+s)R_3]} \quad (12)$$

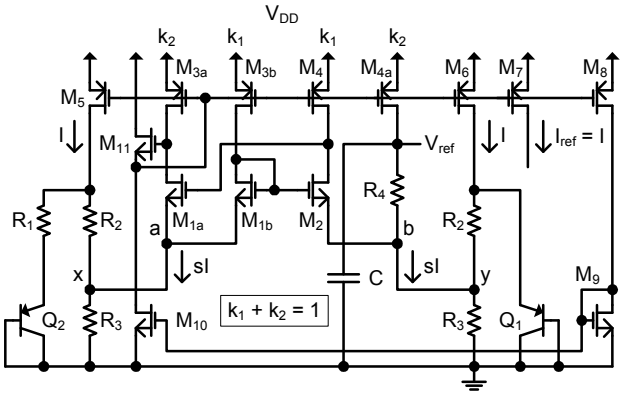

Fig. 5: LV bandgap without using an opamp and providing I_{ref} output

The conditions for V_{ref} and I_{ref} to have zero temperature dependence at $T = T_0$ can be derived as

$$TC_R = \frac{1}{I_{ref}(T_0)}\frac{R_3}{R_1[sk_2R_4 + (1+s)R_3]}\frac{k\ln(N)}{q} \quad (13)$$

$$\left.\frac{\partial V_{EB1}}{\partial T}\right|_{T=T_0} = -G\frac{k\ln(N)}{q} \quad (14)$$

Using Eqn. 10 – 14, $I_{ref}(T_0)$ can be further simplified as

$$I_{ref}(T_0) = \frac{V_{BG0}}{[R_2 + (1+s)R_3](1 - TC_R T_0)} \quad (15)$$

where $V_{BG0} = (V_{EB1} + G\,\Delta V_{EB}) \sim 1.25V$. Eqn. 15 is useful in determining the total required current and/or resistance when designing the bandgap.

As discussed in Section 4, a PTA can be used for replacing M_7 such that I_{ref} can be calibrated if an absolute accuracy is required for I_{ref}. Since most of the biasing currents in the bandgap are used for generating I_{ref} and V_{ref} directly, lower power consumption can be achieved when compared to the bandgap discussed in Section 3 and the bandgap shown in Fig. 4.

6. Simulation Results

Since the proposed bandgaps shown in Fig. 4 and 5 have similar properties, only the one shown in Fig. 5 was designed to demonstrate the proposed techniques due to its simplicity. It was designed based on a conventional 0.18µm CMOS process, which provides parasitic PNP transistors, 1.8V MOSFETs, as well as 3.3V MOSFETs for I/O circuits. The nominal V_T's were ~0.5V and ~0.7V for the 1.8V MOSFETs and the 3.3V MOSFETs, respectively. P+ diffusion layer without silicide was used for realizing the resistors. The sheet resistance is 133±19Ω/square. The first and the second order temperature coefficients were $1.43\times10^{-3o}K^{-1}$ and $7.82\times10^{-7o}K^{-2}$, respectively. The emitter area ratio, N, was set to 8. The values for s and k_2 were selected to be 0.5 and 0.25, respectively. The capacitor C for filtering high frequency noise was selected to be 0.5pF. Self-cascode technique had been employed for all the PMOSs to increase the output impedance. For a 1V supply, the nominal values of V_{ref} and I_{ref} were designed to be 0.3973V and 2.033µA, respectively. The current consumption excluding the current output was 7.1µA. The proposed bandgap was simulated for different process corners and sheet resistance variations over a temperature range of –20°C and 100°C. The results for V_{ref} and I_{ref} are shown in Fig. 6 and 7, respectively. The maximum temperature coefficients of V_{ref} and I_{ref} for different process corners and sheet resistance variations were found to be < 21ppm/°C and < 45ppm/°C, respectively. The overall % changes on V_{ref} ranged between –0.44% and 0.53%. The absolute accuracy on the current output depends on the variations of the resistors as discuss above. For different process corners, the power supply rejection measured at V_{ref} was greater than 42.5dB at 1kHz as shown in Fig. 8. The worst case line regulations for V_{ref}

and I_{ref} were found to be < 3.78mV/V and < 4.45nA/V, respectively. The bandgap operate correctly for V_{DD} > ~0.85V at room temperature. Based on the simulation results, it was demonstrated that the proposed bandgap can also provide a temperature compensated reference current output at a low supply voltage, in addition to the reference voltage output. The bandgap is also robust against supply voltage and process variations.

7. Summary and Conclusion

In this paper, low voltage bandgap reference design techniques that can generate both a reference voltage output, V_{ref}, and a temperature compensated reference current output, I_{ref}, simultaneously were proposed. The first technique used a bandgap core to compensate for the resistor temperature dependence. V_{ref} was then obtained by modifying the output load. The second technique merged the modified load into the bandgap core such that V_{ref} and I_{ref} can be temperature compensated separately with proper selection of resistor values. The second technique is more attractive since fewer components are required. Based on this technique, a low voltage bandgap without using an opamp was designed based on a conventional 0.18µm CMOS process. For a 1V supply, the overall % changes on V_{ref} due to temperature, process and sheet resistance variations were < 0.53%. The temperature coefficients of V_{ref} and I_{ref} were < 21ppm/^{o}C and < 45ppm/^{o}C, respectively. The proposed bandgap is relatively simple and easy to design. Hence, it can be used in many low voltage analog and digital ICs, especially for sensor applications.

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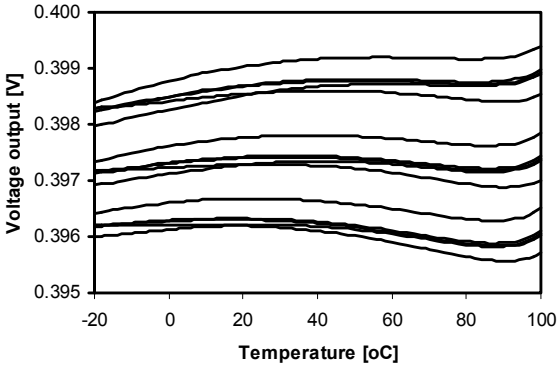

Fig. 6: V_{ref} vs. temperature for different process corners and sheet resistance variations

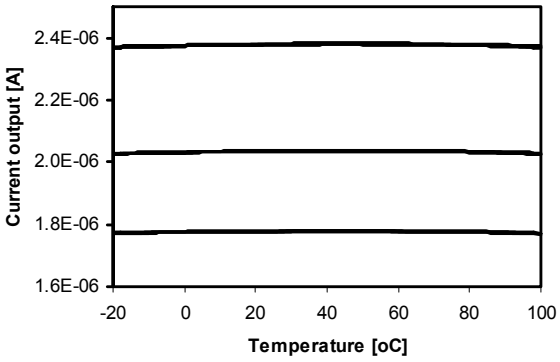

Fig. 7: I_{ref} vs. temperature for different process corners and sheet resistance variations

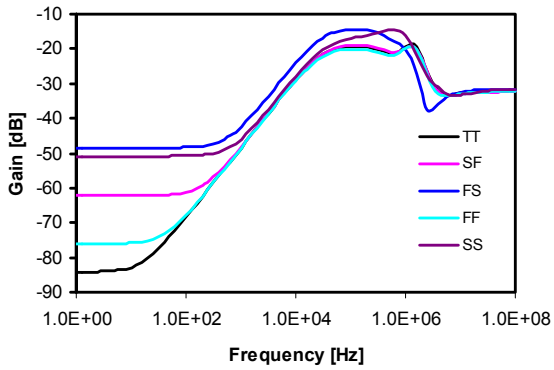

Fig. 8: Voltage gains between V_{DD} and V_{ref} for different process corners